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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,232	02/27/2004	Ronald O. Smith	2207/1012802	4803

23838 7590 12/15/2005

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,232	SMITH, RONALD O.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 16-30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,708,284. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

3. Regarding claim 16:

a. Regarding the limitation of "at least two processors, each processor including a plurality of pipeline stages for processing at least some of the same instructions," the patent claims, in claim 1, "at least two processors, each processor including a plurality of pipeline stages for processing the same instructions." It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the application and the patent claim the same functionality in the claims. The language off "at least some of the same," found in the application, is equivalent to the language of "the same," found in the patent.

b. Regarding the limitation of "wherein each pipeline stage includes a parity bit generator to generate at least one parity bit for each pipeline stage," the patent claims "wherein each pipeline stage includes a parity bit generator to generate at least one parity bit for each pipeline stage," which are the same limitation.

c. Regarding the limitation of "a comparing circuit to compare the parity bit of a stage of one of the at least two processors to the parity bit of the same stage of another of the at least two processors and indicate an error when the parity bits are different in value," the patent claims "a comparing circuit intercoupled to the processors, the comparing circuit comparing the parity bit of a stage one processors to the parity bit of the same stage of another processor, and indicate an error when the parity bits are different in value." It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the application and the patent claim the same functionality in the claims. The language off "at least some of the same," found in the application, is equivalent to the language of "the same," found in the patent.

4. Regarding claims 17-20, the claims are the same language as claims 2-5 in the patent.

5. Regarding claim 21:

d. Regarding the limitation of "processes at least some of the same instructions for at least two processors," the patent claims, in claim 6, "process the same instructions for at least two processors." It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the application and the patent claim the same functionality in the claims. The language off "at least some of the same," found in the application, is equivalent to the language of "the same," found in the patent.

e. Regarding the limitation of "compare at least one parity bit of a first pipeline stage for one processor with at least one parity bit of a second pipeline stage of another

processor performing a similar function as the pipeline stage," the patent claims "compare at least one parity bit of a pipeline stage for one processor with at least one parity bit of the same stage of another processor." It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the application and the patent claim the same functionality in the claims. The language off "a first... a second... performing a similar function as the pipeline stage," found in the application, is equivalent to the language of "the same," found in the patent.

f. Regarding the limitation of "indicate an error when the parity bits are different in value," the patent claims "indicate an error when the parity bits are different in value." The limitations are the same.

6. Regarding claims 22-25, the claims are the same language as claims 7-10 in the patent.

7. Regarding claim 26:

g. Regarding the limitation of "a memory storing a plurality of instructions; at least two processors, each processor coupled to said memory and including a plurality of pipeline stages for processing at least some of the same instructions from said memory," the patent claims, in claim 11, "processing the same instructions during a plurality of pipeline stages fro at least two processors." It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the application and the patent claim the same functionality in the claims. The language off "at least some of the same," found in the application, is equivalent to the language of "the same," found in the patent.

h. Regarding the limitation of "wherein each pipeline stage includes a parity bit generator to generate at least one parity bit for each pipeline stage," the patent claims "generating at least one parity bit for each pipeline stage," which are the same limitation.

i. Regarding the limitation of "a comparing circuit to compare the parity bit of a stage of one of the at least two processors to the parity bit of the same stage of another of the at least two processors and indicate an error when the parity bits are different in value," the patent claims "comparing the parity bit of a stage one processors to the parity bit of the same stage of another processor; and indicate an error when the parity bits are different in value." It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the application and the patent claim the same functionality in the claims. The language off "at least some of the same," found in the application, is equivalent to the language of "the same," found in the patent.

8. Regarding claims 27-30, the claims are the same language as claims 12-15 in the patent.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

10. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

11. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

14. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

Tim Bonura
Examiner
Art Unit 2114

tmb
December 12, 2005

SCOTT BADERMAN
PRIMARY EXAMINER